Total Ionizing Dose Effects on a Radiation Hardened CMOS Image Sensor Demonstrator for ITER Remote Handling

Vincent Goiffon, *Member, IEEE*, Serena Rizzolo, *Member, IEEE*, Franck Corbière, Sébastien Rolando, Said Bounasser, Marius Sergent, *Student Member, IEEE*, Aziouz Chabane, Olivier Marcelot, *Member, IEEE*, Magali Estribeau, *Member, IEEE*, Pierre Magnan, *Member, IEEE*, Philippe Paillet, *Senior Member, IEEE*, Sylvain Girard, *Senior Member, IEEE*, Marc Gaillardin, *Member, IEEE*, Claude Marcandella, Timothé Allanche, Marco Van Uffelen, *Member, IEEE*, Laura Mont Casellas, Robin Scott and Wouter De Cock

***Abstract*—Total Ionizing Dose (TID) effects are studied on a radiation hardened by design (RHBD) 256x256-pixel CMOS image sensor (CIS) demonstrator developed for ITER remote handling by using X and γ-rays irradiations. The (color) imaging capabilities of the RHBD CIS are demonstrated up to 10 MGy(SiO_2), 1 Grad(SiO_2), validating the radiation hardness of most of the designed integrated circuit. No significant sensitivity (i.e. responsivity and color filter transmittance) or readout noise degradation is observed. The proposed readout chain architecture allows achieving a maximum output voltage swing larger than 1 V at 10 MGy(SiO_2). The influence of several pixel layout (the gate oxide thickness, the gate overlap distance and the use of an in-pixel P+ ring) and manufacturing process parameters (photodiode doping profile, process variation) on the radiation induced dark current increase is studied. The nature of the dark current draining mechanism used to cancel most of the radiation induced degradation is also discussed and clarified.**

***Index Terms*—ITER, CMOS Image Sensors, CIS, Active Pixel Sensors, APS, Image Sensors, Radiation Hard, Rad Hard, Radiation Tolerant, Monolithic Active Pixel Sensor, MAPS, Ionizing Radiation, Total Ionizing Dose, TID, MGy, Grad, Gigarad, Megagray, MGy, Dark Current, Quantum Efficiency, Enclosed Layout Transistors, ELT, Radiation Hardening, RHBD, Interface States, Trapped Charge, Shallow Trench Isolation, STI, Deep Submicron Process, DSM, CMOS, Integrated Circuit, Radiation Effects, Radiation Damage, X-rays, gamma-rays, Co60.**

I. Introduction

Solid-state high definition and color optical imagers with radiation hardness well above a Total Ionizing Dose (TID) of 1 MGy(SiO2), i.e. 100 Mrad, are required for the development of critical remote handling systems in ITER fusion reactor. The availability of such rad-hard imager would also completely transform the way remote handling and monitoring are performed in highly radioactive environments, by increasing operational efficiency, but also by reducing risks, costs and the frequency at which cameras are replaced. It would also enable the inspection of radioactive areas that cannot be observed today. Typical applications that would greatly benefit from this solution are remote handled maintenance, monitoring and inspection operations in many nuclear facilities—such as nuclear power plants, nuclear storage waste repositories, particles physics and irradiation facilities —as well as mobile rescue robots.

Space applications could also benefit significantly from optical image sensors with TID tolerance beyond 100 Mrad. This is for example the case for future missions to Jupiter's moon, such as Europa and Io, where 100 Mrad / 1 MGy rad-hard electronics would greatly reduce the required amount of shielding [1].

Previous work has demonstrated that reaching a 10 MGy (1 Grad) radiation hardness with a CMOS Image Sensor (CIS) is feasible [2], [3]. In order to confirm this conclusion and to demonstrate that a full camera can also be made radiation hard up to several Mega-gray, the FUsion for energy Radiation Hard Image sensor (FURHI) and Imaging System (FURHIS) demonstrators have been developed. The FURHIS camera is comprised of the FURHI CIS, a radiation hardened optical system and a radiation hardened illumination system [4].

This paper focuses on the FURHI CIS performances. The purpose of this work is to find original techniques to improve the performances of radiation hardened CIS after exposure to high level of TID (up to 10 MGy, 1 Grad) by exploring new design and technology variations. In particular, this study focuses on:

- studying the radiation hardness of CIS analog functions based only on 3.3V N-channel MOSFETs;
- comparing the radiation hardness of shallow and deep CIS photodiodes;
- clarifying the influence of gate oxide thickness on the radiation hardness of gate-overlap photodiode designs;
- confirming and optimizing the dark current cancellation mechanism reported in [3].

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V. Goiffon, S. Rizzolo, F. Corbière, S. Rolando, S. Bounasser, M. Sergent, A. Chabane, O. Marcelot, M. Estribeau and P. Magnan are with ISAE-SUPAERO, Université de Toulouse, Image Sensor Research Team, 10 avenue E. Belin, F-31055, Toulouse, France.

S. Girard and T. Allanche are with Université de Saint-Etienne, Laboratoire Hubert Curien, UMR-CNRS 5516, France.

P. Paillet, M. Gaillardin and C. Marcandella are with CEA, DAM, DIF, F-91297 Arpajon, France.

M. Van Uffelen and L. Mont Casellas are with Fusion for Energy (F4E), c/Josep Pla, n° 2, Torres Diagonal Litoral, Ed. B3, 08019 Barcelona, Spain.

R. Scott is with Oxford Technologies Ltd.(OTL), 7 Nuffield Way, Abingdon OX14 1RL, UK.

W. De Cock is with SCK-CEN, Boeretang 200, 2400 Mol, Belgium.

Table I
SUMMARY OF THE TARGETED FULL SIZE PROTOTYPE PERFORMANCES.

Feature/Parameter	Target
Pixel array size	1280×720
Pixel pitch	10 μm
Color	yes
Frame rate	25 fps
ADC resolution	10 bits
Failure TID	> 1 MGy(SiO_2)
Failure dose rate	> 100 Gy(SiO_2)/h

A secondary objective is to clarify further the influence of irradiation conditions, i.e. biasing conditions (ON vs OFF) and particle type (X-rays vs γ-rays), on the achieved radiation hardness.

After the presentation of the demonstrator details and irradiations conditions in section II, the radiation test results are reported and discussed in the third part of this manuscript. This paper is concluded by an extended discussion on the dark current draining mechanism and the possibilities for further design improvements (section IV), before the final summary and conclusion.

II. Experimental details

A. The FURHI Sensor

During its operational phase, several neutron-activated components of ITER exposed to the fusion plasma harsh environment will have to be replaced. These maintenance activity phases will last for 6 months, during which the plasma is turned OFF. The replacements will involve cutting and soldering pipes, for which several viewing systems will be required to monitor the remote handling operations and even assist with weld inspections [5]. For such operations, the radiation environment will mainly consist of gamma rays (^{60}Co) emitted by the activated materials – mainly stainless steel – during ITER operations. Hence, the primary challenge to meet for this camera development is the TID requirement. For this reason, this study focuses only on TID effects. Accurate neutron flux and fluences determination is on-going and Single Event Effects (SEE) in this CIS architecture will be the subject of future work. The influence of displacement damage on the CIS performances is expected to be completely hidden by the TID induced degradation but, as for SEE, this will also be verified in a future step of the development.

The targeted specifications for the full format radiation hard camera-on-a-chip required for ITER remote handling operation (such as pipe weld inspection) is summarized in Tab. I. The "failure dose rate" mentioned in the table represents the dose rate that the final camera-on-a-chip shall be able to withstand with no failure or critical image quality degradation. There is no single event effect (SEE) or displacement damage dose specification since, in this particular case, the main radiation source is the gamma ray field as mentioned before. The sensor sensitivity is not specified a priori either since it will be the consequence of other design and manufacturing choices. The illumination system power and the sensor integration time will be tuned to achieve the sensitivity required by the application at the camera level. It is worth noting that the final

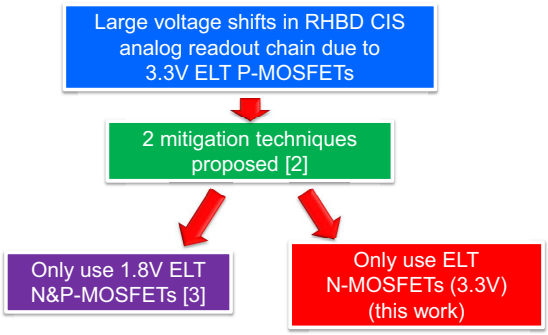

Figure 1. Overview of the explored radiation hardening approaches for the CIS analog readout chain.

radiation hardened camera-on-a-chip integrated circuit will embed all the required electronics to acquire and transmit the "digital" images whereas the FURHI demonstrator integrates only the elementary functions required to capture"analog" frames (i.e. a pixel array, decoders, readout chains, sample-and-hold stages and multiplexers). The radiation hardness of a more integrated camera-on-a-chip with an on-chip sequencer and Analog-to-Digital Converters (ADC) will be studied in a next step. However, the results previously obtained on digital circuits and ADC test structures [3] on the same technology suggest that reaching the required radiation hardness for the full camera-on-a-chip is possible.

The FURHI CIS demonstrator was manufactured using a 180 nm CIS process with dedicated photodiode profiles and optimized in-pixel devices using a Multi Project Wafer (MPW) access managed by imec-europractice. Since by essence a MPW is shared by several customers, it is not always possible to choose and define all the process conditions and thus, some process variations may appear from one lot to another. This was used in the FURHI project as an indirect way to evaluate the sensitivity of the proposed Radiation-Hardening-By-Design (RHBD) techniques on the process variations. The integrated image sensor itself is comprised of 256×256 pixels with three transistors per pixel and a pitch of 10 μm. The whole circuit is radiation-hardened-by-design [6], especially by using enclosed geometries (Enclosed Layout Transistors (ELT) [7]) for all N and P MOSFETs (1.8 V and 3.3 V ones) to mitigate Radiation Induced Narrow Channel Effect (RINCE) [8], sidewall leakages and junction leakages. In previous explorations [2], [3], it appeared that 3.3 V P channel transistors were too sensitive to TID to be used beyond 100 kGy because of large gate oxide trapped charge induced threshold voltage shifts (ΔV_{ot}). On the other hand 3.3 V N-channel transistors did not exhibit any ΔV_{ot} after several MGy and their threshold voltage was only influenced by a limited interface state induced shift (ΔV_{it}) [2]. Such enhanced sensitivity of P-channel MOSFETs has been reported on several technology nodes and foundries [9]–[11] and its root cause, that seems to differ from one node to another, is still under investigation.

As summarized in Fig. 1, two mitigation options have been proposed to design the analog function of the RHBD CIS without suffering from the 3.3 V P-MOSFET degradation. The first one is to design a full 1.8 V CIS with no use of double

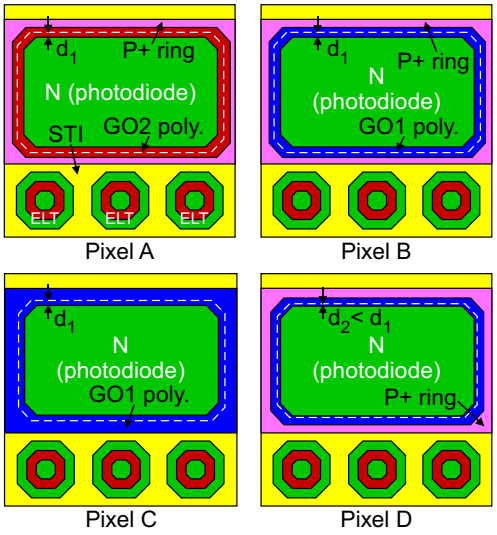

Figure 2. Top view illustration of the four pixel designs used in FURHI to highlight the influence of the photodiode design parameters on its radiation hardness. The distance d is the as-drawn overlap distance between the gate and photodiode N doping. GO1 (in blue) = simple gate oxide (used in 1.8 V transistors). GO2 (in red) stands for double gate oxide (used in 3.3 V transistors). Shallow Trench Isolation are represented in yellow. P+ rings are drawn in pink and N doped regions in green. ELT = Enclosed Layout Transistor.

gate oxide (GO2). This solution has been explored in [3]. The second one, which has been selected for the FURHI project, is to base the analog design exclusively on 3.3 V N channel transistors.

The FURHI pixel array is divided into eight regions to study the response of four different pixel designs (shown in Fig. 2), all based on the gate overlap design proposed in [2], with and without a color filter array (CFA) on top of them (to confirm the high radiation hardness of CFA). It should be emphasized that FURHI pixel A design is exactly the same as the pixel C design in [2] (i.e. the gate overlap layout) and it will be referred to as pixel A design from [2] in this manuscript for the sake of clarity. Two versions of FURHI (illustrated in Fig. 3) have been manufactured: FURHI_D use a deep photodiode doping profile whereas FURHI_S use a shallow photodiode doping profile. Thanks to this doping variation and to the two different gate oxide thicknesses used in FURHI pixels (pixel A vs the others), it is possible to clarify which one of these differences allowed to reduce by an order of magnitude the radiation induced dark current in [3].

Pixel design variations only had a significant influence on the dark current, the four pixels exhibited comparable performances for the other studied parameters. For this reason, if not stated otherwise, the presented results (other than dark current) have been measured on FURHI_D pixel C.

B. Irradiation Details

The room temperature irradiation conditions are summarized in Tab. II. γ-ray irradiations were performed at SCK-CEN (dose rate ≈ 700 Gy/h) whereas X-ray exposures were done at CEA, DAM, DIF (dose rate ≈ 180 kGy/h). The ON condition refers to sensors biased and operated with nominal sequencing signals (continuous frame acquisition). The OFF

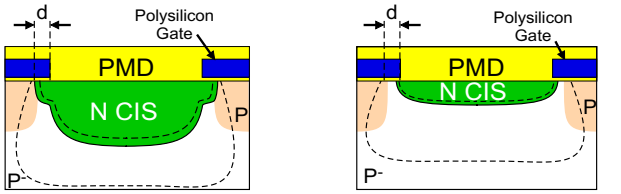

Figure 3. Cross sectional view illustration of the deep and shallow diode doping profiles on the pixel C design. The as-drawn overlap distance d is represented to show that the deep diode is influenced by d whereas the shallow diode is self-aligned on the polysilicon gate, whatever the d value (if d is positive). PMD = Pre-Metal Dielectric.

Table II
IRRADIATION CONDITIONS SUMMARY.

CIS ID	Diode profile	Irradiation conditions	TID steps (MGy)
FURHI_D_1	Deep	^{60}Co γ-ray, ON	0.4 ; 1
FURHI_D_2		^{60}Co γ-ray, ON	0.4 ; 1
FURHI_D_3		^{60}Co γ-ray, OFF	0.4 ; 1
FURHI_D_4		^{60}Co γ-ray, OFF	0.4 ; 1
FURHI_D_5		10 keV X-ray, OFF	2 ; 5 ; 10
FURHI_D_6		10 keV X-ray, ON	1
FURHI_D_7		10 keV X-ray, OFF	1
FURHI_D_8		10 keV X-ray, OFF	0.001
FURHI_D_9		10 keV X-ray, OFF	0.01
FURHI_D_10		10 keV X-ray, OFF	0.01 ; 0.1
FURHI_S_1	Shallow	^{60}Co γ-ray, ON	0.1
FURHI_S_2		^{60}Co γ-ray, ON	0.1
FURHI_S_3		^{60}Co γ-ray, OFF	0.1 ; 0.5 ; 1.1
FURHI_S_4		^{60}Co γ-ray, OFF	0.1 ; 0.5 ; 1.1

condition means that the sensors are fully grounded. The static bias case is not considered for CIS testing since it is completely unrealistic and since it would lead to leave floating important areas of the sensor (such as the photodiodes). The variability from one chip to another exposed to the same irradiation condition was very low for most of the parameters. Therefore, in the following, the irradiation conditions are recalled only if a significant difference was observed. If not, the average measured value is reported.

If not stated otherwise, the measurements have been performed between four days and two weeks after the end of the ^{60}Co irradiation and between one day and one week after X-ray exposure. No significant variation of the measured parameters that could change the analysis and conclusion of this study has been observed on this timescale (i.e. from one day to two weeks after irradiation, room temperature annealing had a negligible impact on the measured data). All the radiation doses are given in Gy(SiO_2) (or rad(SiO_2)) in this article.

III. Radiation Test Results

All the results presented in this section were measured in a temperature regulated dark room at $22°C \pm 0.5°C$.

A. Imaging capabilities

The capability of the studied image sensor to capture images after exposure to 10 MGy(SiO_2), 1 Grad(SiO_2), of TID is illustrated in Fig. 4. These color images demonstrate that the sensor is properly functioning and they validate the radiation

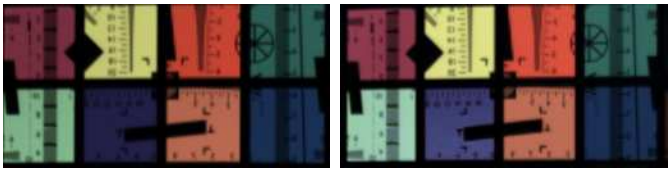

Figure 4. Color image captured by FURHI_D_5 before irradiation and after 10 MGy(SiO_2).

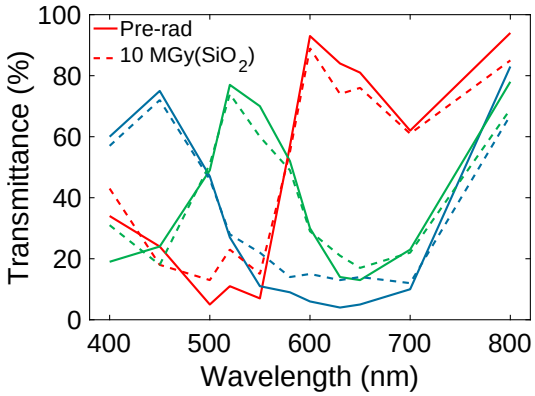

Figure 5. Color filter array transmittance measured on FURHI_D_5 before and after exposure to 10 MGy(SiO_2).

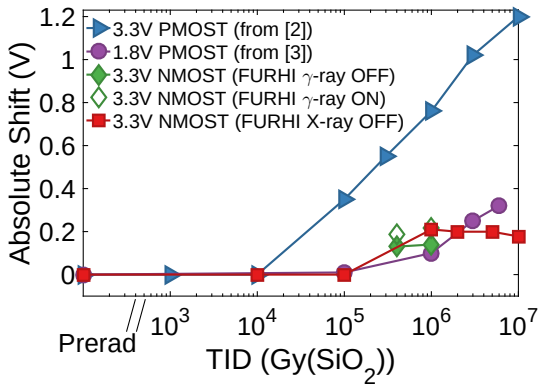

Figure 6. Comparison of the absolute voltage shift of the CIS output stage MOSFET current source for several transistor technologies.

hardness of the multiple digital circuits used in this CIS design. This figure also shows that the color rendering is weakly influenced by ionizing radiation, as concluded in [3] at a lower TID. The transmittance of the color filter array presented in Fig. 5 provides a quantitative confirmation that even at 10 MGy(SiO_2), the radiation induced degradation of CMOS color filter arrays is not significant.

B. Analog Readout Chain

Fig. 6 presents the absolute radiation induced voltage shift measured on the MOSFET used as a current source in the output stage of the CIS for several cases (depending on the sensor architecture, as illustrated in Fig. 1). It recalls that 3.3 V P-MOSFETs suffer from very large voltage shifts and should be avoided. As discussed in [3], using 1.8 V P-MOSFETs instead delays the degradation toward higher

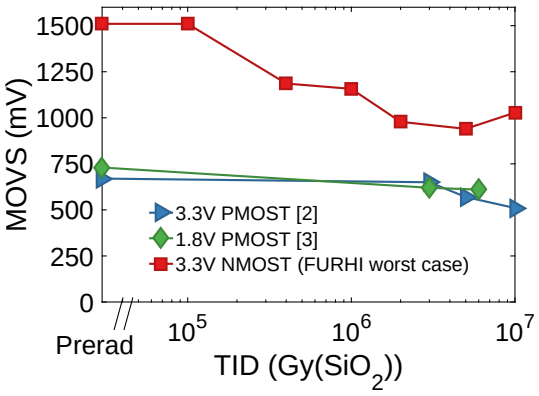

Figure 7. Maximum Output Voltage Swing (MOVS) evolution with TID for the three studied readout chain architectures.

TID but a continuous shift appears at 1 MGy and beyond. On the contrary, despite a much thicker gate oxide, FURHI output stage 3.3 V N-MOSFETs exhibit a reasonable shift which saturates quickly and allows reaching stable electrical performances in the 1-10 MGy range.

A first effect of biasing conditions can be seen on FURHI γ-ray data at 0.4 and 1 MGy. As usually stated in literature [12], the ON case enhances the N-MOSFET degradation but the difference with OFF condition is reasonable ($\approx 20\%$). Comparable weak enhancement has been reported in [3] and no visible effect of biasing conditions was seen on the 3.3 V N and P architecture [2]. Hence, it can be concluded that the ON case is confirmed as the worst case for testing the MOSFET part of the sensor but the difference with the OFF case is weak enough to consider the OFF case as a relevant condition for exploration. The X-ray OFF data are in good agreement with γ-ray ON irradiations but they are above the grounded γ-ray case. This is most likely due to the difference in dose rate (and thus to the difference in total "biased" annealing time) since 1 MGy was deposited in a working day with X-rays whereas two one-month-irradiations were necessary to reach the same TID with ^{60}Co. So it can be concluded that, X and γ-ray irradiations results are in good agreement.

The effect of individual MOSFET voltage shift on the Maximum Output Voltage Swing (MOVS) of the sensor (which gives the sensor dynamic range performance) is not straightforward and depends on several factors related to the readout chain architecture. Indeed, as presented in previous work [2], [3], when the MOSFET threshold voltage is shifted by a given voltage, the analog electrical transfer function is generally shifted by a comparable value but the useful voltage swing is not necessarily reduced. It is thus necessary to plot the evolution of MOVS with TID (as presented in Fig. 7) to conclude which solution is the most efficient mitigation technique at the sensor level. This figure shows that the FURHI architecture MOVS decreases with TID up to 2 MGy and then stabilizes at a fairly high MOVS ($\approx$ 1 V), whereas the previous generation of sensors exhibits a reduced MOVS that is continuously decreasing in the 1-10 MGy range, reaching half the MOVS of the FURHI sensor at 10 MGy. Hence, using 3.3 V N-MOSFETs only for the analog functions appears to be an efficient mitigation technique.

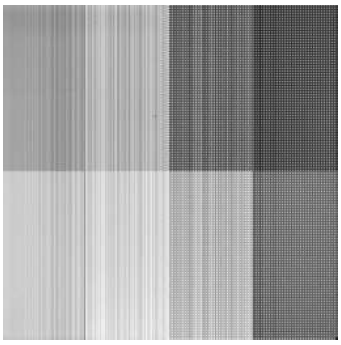

Figure 8. Raw image captured with FURHI_D after the absorption of 1 MGy under uniform and static illumination ($\lambda = 650$ nm) illustrating the important column Fixed Pattern Noise due to the radiation induced NMOSFET variability. The grid pattern on the right side of the picture is due to the response of the color filter array to monochromatic illumination.

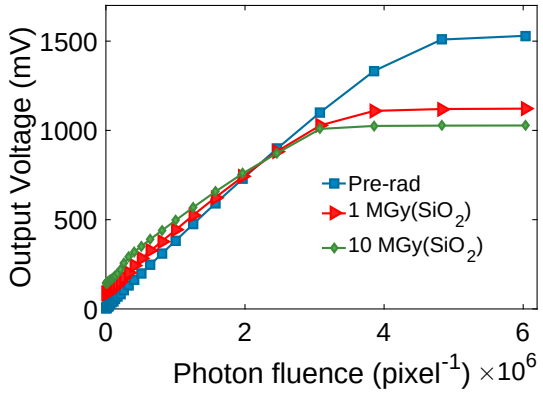

Figure 9. Average opto-electrical transfer function (at $\lambda = 650$ nm) measured on pixel C before irradiation, at 1 MGy(SiO_2) and at 10 MGy(SiO_2).

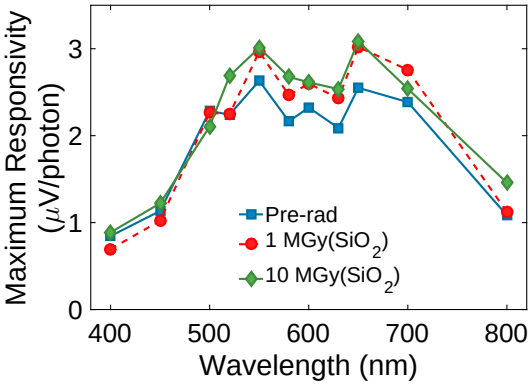

Figure 10. Maximum responsivity measured on pixel C before irradiation, at 1 MGy(SiO_2) and at 10 MGy(SiO_2).

However, a non-ideality appeared on this particular sensor after exposure to a few hundreds of kilograys: an important Fixed Pattern Noise (FPN) due to an unexpected large variability of the 3.3 V N-MOSFETs threshold voltage shifts. This effect is illustrated by the raw image captured under uniform and static illumination conditions presented in Fig. 7. It was not significant enough in the previously studied RHBD sensors to degrade the image quality whereas in the FURHI sensor, an FPN cancellation operation is required to obtain a good quality image. Such cancellation can be as simple as subtracting a raw dark frame (with minimum integration time) to the useful images and such calibration is often done in imaging systems (at least once right after manufacturing) but in the case of this project, the calibration dark frame would have to be acquired several times during the lifetime of the camera. It is worth noting that this effect is not visible in the color image displayed in Fig. 4 because the calibration step (i.e. white balancing) necessary to obtain a color image with a raw sensor cancels this FPN. The root cause of this MOSFET variability is linked to manufacturing process variations and it is further studied and discussed in a companion paper [13]. It is worth noting that comparable enhanced variability of CMOS MOSFETs has been recently reported in this TID range in another CMOS process [11], but the physical origin may differ from one process to another.

Regarding the readout chain noise, in this 3T pixel design, the main noise contribution is the in-pixel kTC noise and the achieved output readout noise value is about 600 μVrms on all the studied sensors. This performance was not significantly degraded by ionizing radiation (less than 100 μVrms increase) suggesting that the photodiode capacitance has not changed much and that the kTC remained the main readout noise source.

C. Opto-Electrical Transfer Function

The radiation induced degradation of the opto-electrical transfer function observed on the FURHI sensor (Fig. 9) at 1 MGy is well in line with previous work: some linearity degradation at the beginning of the curve and a saturation voltage decrease. As mentioned in the previous section, the overall maximum output voltage swing after irradiation is much larger than in the previous sensors. In the first part of the curve, before the strong non-linearity, the slope does not seem degraded, and thus, no obvious change of maximum responsivity can be seen in this figure. However, in the quasi-linear part of the transfer function (approximately between 400 and 700 mV in Fig. 9) a small slope reduction appears demonstrating a slight radiation induced responsivity decrease in the second part of the output voltage range. The maximum responsivity (i.e. maximum slope of the transfer function determined before the non-linearity of Fig. 9) is presented in Fig. 10 before irradiation, after 1 MGy and 10 MGy. The apparent increase in responsivity for some wavelengths is due to the uncertainties related to the non-linearities at low photon fluence in Fig. 9. Despite these uncertainties, it can be concluded that up to 10 MGy there is no critical deterioration (i.e. that the degradation is weaker than 50%) of the spectral response after exposure to this dose of ionizing radiation.

D. Radiation induced dark current increase

The performance parameter which requires extra attention is the dark current level reached in the Megagray range. A high dark current value leads to a reduction of the dynamic range of the sensor by reducing the effective voltage swing, increasing the temporal noise and limiting the range of exposure time that can be used in the camera.

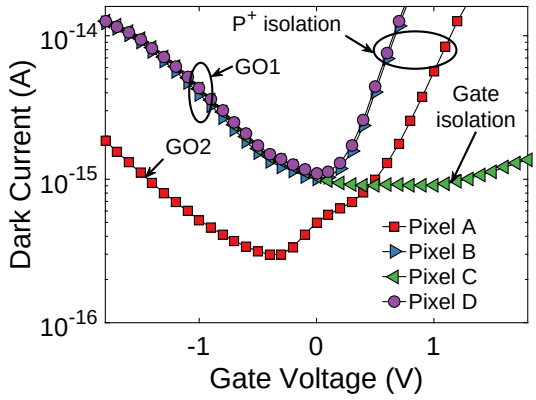

Figure 11. Dark current as a function of gate voltage before irradiation on FURHI_D_1. Temperature = 22°C.

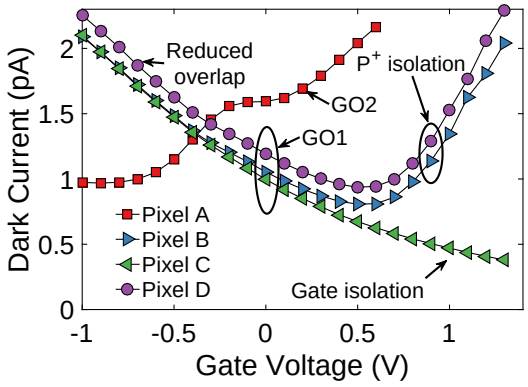

Figure 12. Dark current as a function of gate voltage on FURHI_D_1 after 1 MGy for the four studied pixel designs. Temperature = 22°C.

First, the differences between the designs studied in the FURHI sensor can be seen in Fig. 11 and Fig. 12. These figures show the expected evolution of leakage current with gate voltage in gated diode [2], [14] with an optimum value for pixels with a P+ isolation ring (pixel A, B and D) which generally corresponds to the beginning of hole accumulation. Lower gate voltages than this optimum lead to trap assisted tunneling due to the band bending induced by the gate in the N-region of the photodiode (the so called Gate Induced Drain Leakage (GIDL) phenomenon in MOSFETs [15], [16]). Higher gate voltages than the optimum also increases the dark current through a similar enhancement of the trap assisted generation in pixel A, B and D designs because of the creation of a high electric field region at the boundary between the surrounding and the P+ ring. These two graphs (Fig. 11 and Fig. 12) demonstrate that using a thinner gate oxide does not bring a significant improvement of the minimum dark current value (pixel A versus pixel B) after irradiation and that it even degrades much the leakage current before irradiation. They also show that if the overlap distance is reduced, the dark current rises slightly in the irradiated sensor, confirming the need for a sufficient overlap to properly shield the surface junction. Similar effects were observed on all the dark current measurements of pixel A, B and D for all TID levels and irradiation conditions.

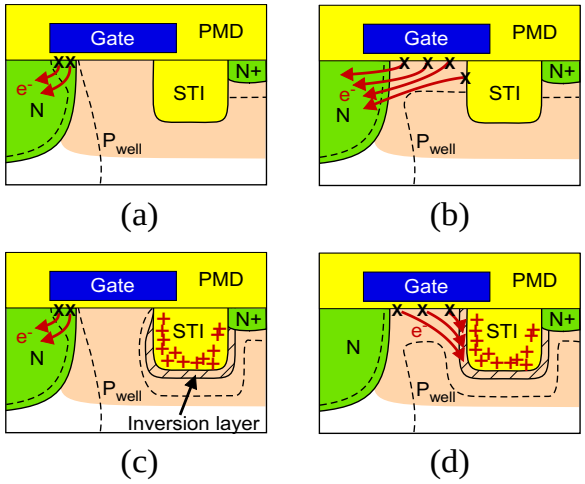

Figure 13. Illustrations of the dark current draining mechanism in pixel C. These drawing corresponds to a vertical cross section in the pixel C layout of Fig. 2. Are represented from left to right: the end of the photodiode, the protective gate, the STI and an ELT outer drain biased to VDD. a) Before irradiation or at low TID with gate under accumulation. b) Before irradiation or low TID with depleted gate. c) High TID with accumulated gate. d) High TID with depleted gate. Black X represent active interface generation centers (i.e. interface states). The hatched region represents the STI trapped charge induced inversion channel.

In pixel C before irradiation (Fig. 11), the dark current stays at its minimum value even for gate voltages larger than the optimum exhibited by the other pixel designs. In this gate voltage range, the gate is depleted and the photodiode depletion region extends toward the Shallow Trench Isolation (STI) sidewall as depicted in Fig. 13(b). Since there is no increase up to 1-1.5 V, it can be inferred that either the STI sidewall is passivated with additional P doping (preventing the depletion region from reaching the STI) or that the interface state density is not large enough on the STI sidewall to induce a visible increase before irradiation.

After exposure to 1 MGy(SiO_2), a continuous dark current reduction for increasing gate voltage appears on the pixel without the P+ ring (pixel C). This dark current cancellation mechanism has already been reported in the RHBD 1.8 V sensor tested in [3]. It can be explained by the cross sectional view of pixel C presented in Fig. 13(d). After a sufficient TID, the STI positive trapped charge leads to the depletion and the inversion of the STI interface. This electron inversion layer is connected to the nearest VDD junctions (the in-pixel ELT outer drains). For sufficiently positive gate voltage, the dark electrons generated by the interface states at the gate oxide interface are more likely to be collected by the STI inversion layer (biased at VDD) than by the photodiode itself (biased several hundreds of mV below VDD). The higher is the gate voltage, the more dark electrons are directed toward the STI inversion channel because of the potential profile below the gate as discussed in [17].

The third graph dedicated to dark current (Fig. 14) compares the evolution of the minimum dark current (i.e. obtained at the optimum gave voltage) with TID of FURHI pixel A, B and C (pixel D curve is similar to the one of pixel C) to the response of pixel design A from a previous manufacturing lot (from [2]). For pixel C, no gate voltage larger than 1.3 V has been used

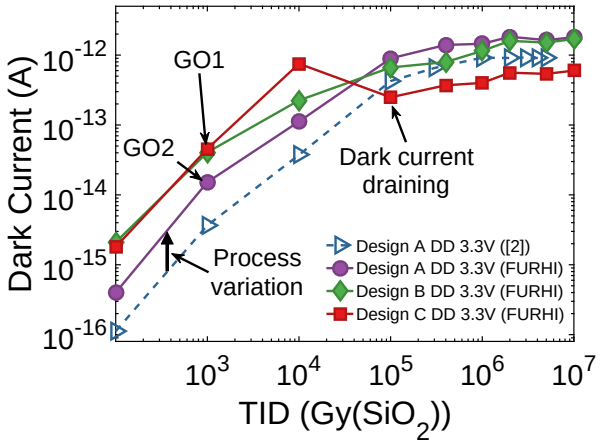

Figure 14. Minimum dark current evolution with TID for FURHI_D pixel A, B and C compared to the results obtained on the same design as pixel FURHI A on a previously manufactured sensor (i.e. the data obtained on the pixel called C in [2]). Temperature = 22°C.

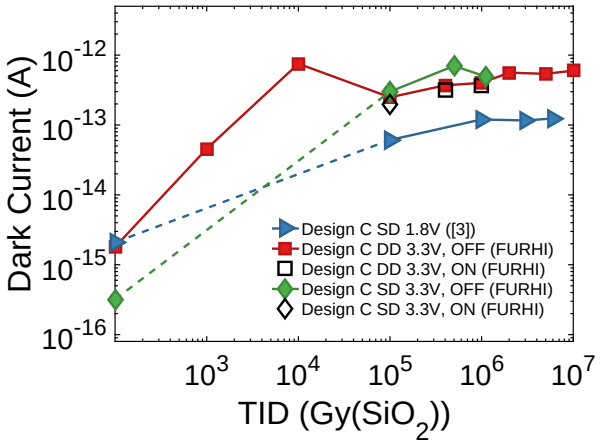

Figure 15. Comparison of the minimum dark current evolution with TID of the FURHI sensors with deep diode and shallow diode, with 3.3V and 1.8V operating voltages and with two biasing conditions during irradiation: ON vs OFF. Temperature = 22°C.

in this study to avoid any risk of electrical cross-talk or even short circuit between adjacent photodiodes.

First, the comparison between the two pixel A designs shows a clear process variation induced dark current increase ranging from a 3X increase before irradiation to 2X in the Megagray range. The root cause of this unwanted effect is not identified yet, but it is not uncommon in MPW access were process conditions can change depending on the different customers' demands. The fact that the dark current is already degraded before irradiation may be used to identify the process variation responsible and to target the right conditions to achieve the best hardness for the full size prototype. Since the purpose of this work is to determine the RHBD technique efficiency on the same technology and process condition, dark current results will not be compared further with [2] and the reader should keep in mind that with the right process conditions, the absolute dark current level achieved with the FURHI demonstrator could possibly be twice better according to Fig. 14.

Second, FURHI pixel A and B evolutions with TID confirm the first conclusion drawn from Fig. 11 and Fig. 12: there is surprisingly no obvious benefit in using thin GO1 oxide to shield the junction, except a slight improvement in the 100 kGy – 1 MGy. Whereas pixel A and B dark currents rise monotonously with absorbed dose, Pixel C exhibits an original behavior: a larger augmentation than B at 10 kGy followed by a significant drop at 100 kGy. This behavior is in agreement with the mechanisms presented in Fig. 13. Indeed, up to 1 kGy, there is no significant difference between pixel B and C, most likely because the STI sidewall passivation is still effective. At 10 kGy, the STI sidewall is depleted and the STI radiation induced interface states bring their important contribution to the total dark current (as illustrated in Fig. 13(b)), leading to a higher dark current in pixel C than in pixel B. Finally, at 100 kGy, the STI radiation induced positive trapped charge is sufficient to create an inversion channel all along the STI interface, thus turning on the dark current draining mechanism (see Fig. 13(d)). Beyond this TID, dark current draining allows the reduction of the pixel dark current in pixel C by a factor of 3 – 4 compared to design A and B (on the same process), hence this design remains the best RHBD solution for the Megagray range.

Fig. 15 compares the evolution of pixel C dark current with TID for the two studied photodiode doping profiles (deep versus shallow diodes), two supply voltage and ON/OFF irradiation conditions. It shows that whatever the design and the technology, dark current always saturates beyond 500 kGy – 1 MGy as also observed on very different CMOS processes [18]. As for the N-MOSFET voltage shift, this stabilization in the Megagray range is a strong benefit for the use of radiation hardened CIS at dose levels reaching and even possibly exceeding 10 MGy (1 Grad). Both phenomena are most likely correlated and due to the same saturation interface state densities in N-polysilicon gate oxide.

As regards the difference between the shallow (SD) and the deep (DD) diodes on 3.3 V pixels, the comparison highlights that the shallow implant alone does not reduce the radiation induced dark current, it even worsens it. Additional measurements (not shown here) highlighted that the shallow diode used with 3.3 V operating voltage suffers from high Electric Field Enhancement (EFE) effects (i.e. a strong dependence on reset supply voltage). This EFE is the reason why the 3.3 V shallow diode is much leakier than the 1.8 V shallow diode. With the full picture in mind, it can be concluded that the reason why the 1.8 V shallow diode is exhibiting the best dark current value in the Megagray range (around ≈ 0.1 pA) is not due to the reduction of oxide thickness but to the use of this shallow implant, as far as low operating voltages are used.

Finally, this figure also informs on the effect of biasing conditions during irradiation. As concluded many times in CIS literature, biasing conditions have little effect on the radiation induced dark current increase of the deep diode pixels (as illustrated by pixel C ON and OFF results). These results show that the ON condition can even improve the dark current, as illustrated by the 3.3 V shallow diode at 10 kGy, which benefits from a self-annealing mechanism due to the EFE induced intense leakage current. This self-annealing process

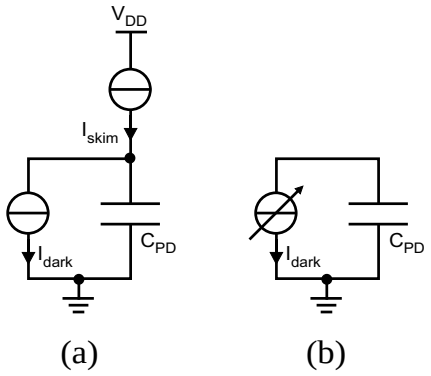

Figure 16. Electrical model of the photodiode during integration showing the fundamental differences between the two dark current reduction techniques discussed here: a) a dark current skimming technique and b) the dark current draining mechanism.

is also the most probable cause of the decrease exhibited by this sensor between 0.5 MGy and 1.1 MGy.

IV. Discussions

A. Dark current reduction mechanism

As discussed in the previous section, when the protective gate is connected to an N+ VDD drain (through the STI inversion here), the dark charge generated at the gate oxide interface can be drained out, hence reducing the dark current. This mechanism is fundamentally different from dark current compensation techniques that are used in imaging, especially in infrared detectors such as skimming, background compensation and other offset correction techniques which only shift the dark current (or the dark signal) without really canceling the generation of dark charges. If the dark current (or the dark signal) is simply shifted (by correcting an offset) dark current associated temporal (shot noise) and spatial (dark current signal non-uniformity (DCNU)) noises are not reduced. Worse, these two noises are generally increased since the skimming technique brings its own noise contribution (temporal and spatial).

For example, in a current skimming technique (e.g as proposed in [19]), an additional current source is used to compensate part of the discharge induced by the dark current (as illustrated in Fig. 16(a)). In this case, by considering that the main readout noise contribution is the hard reset noise [20], that the skimming current is provided by a MOSFET operating in subthreshold and that the readout gain is unitary, the total pixel output noise in Vrms after integration and differential sampling can be expressed:

$$\sigma_{\mathrm{Vout}} = \frac{1}{C_{\mathrm{pd}}}\sqrt{q\left(|I_{\mathrm{dark}}| + |I_{\mathrm{skim}}|\right) \times t_{\mathrm{int}} + 2kTC_{\mathrm{pd}}} \quad (1)$$

with I_{dark} the dark current, I_{skim} the skimming current, t_{int} the integration time, C_{pd} the photodiode capacitance, k the Boltzmann constant, T the absolute temperature and q the elementary charge. This equation shows that the skimming current increases the total noise and that it cannot lead to any noise reduction.

Fig. 17 presents the evolution of the output noise σ_{Vout} of pixel C with the deep diode (at 1.1 MGy). It can clearly be

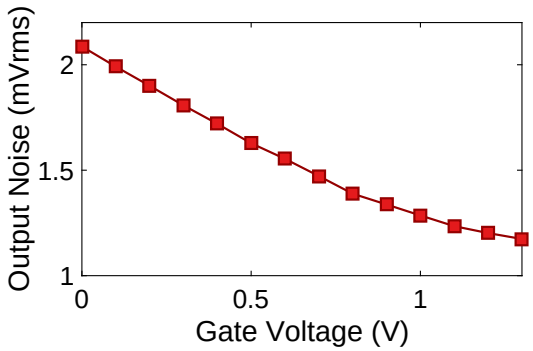

Figure 17. Measured output voltage noise on FURHI_D_1 pixel C at 1 MGy as a function of the gate voltage with an integration time of 30 ms. Temperature = 22°C.

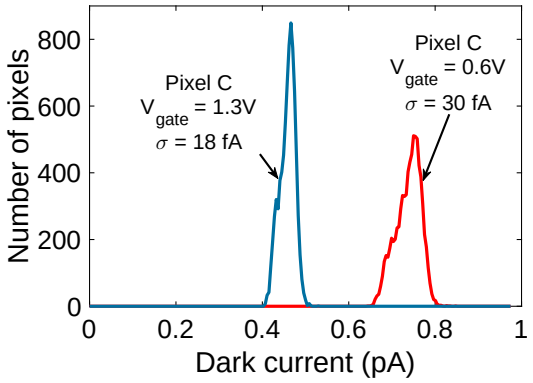

Figure 18. Dark current distributions measured on FURHI_D_1 pixel C at 1 MGy for two different gate voltages (in the dark current draining region) to emphasize the DCNU reduction (i.e. the decrease in standard deviation). Temperature = 22°C.

seen that the total noise decreases with increasing gate voltage (and thus with decreasing dark current) even in the 0.5 − 1.3 V range where the dark current draining is enabled. A similar result is obtained on the DCNU in Fig. 18 which shows a narrowing of the distribution. These two evidences of noise reduction with dark current demonstrate that the dark charges are not integrated by the photodiode and that it is effectively canceled. Hence, the equivalent schematic representing this mechanism is the one displayed in Fig. 16(b), a variable dark current source and not a current offset compensation (as the one illustrated in Fig. 16(a)).

B. Possibilities for Pixel Design Improvements

To benefit further from the dark current reduction mechanism and to control it, it could be possible to enable it on purpose by adding an N+ drain beside the polysilicon gate and by possibly interrupting the polysilicon gate between two adjacent photodiodes to allow the use of higher gate voltage without risking a short circuit between pixels. By doing so, the onset of the dark current draining mechanism would not rely on the STI inversion anymore and thus, it would not be dependent on the TID nor on the annealing history of the irradiated sensor anymore. Such a pixel design has already been manufactured, irradiated and studied in the past (ELD design in [21]), but the biasing conditions that enables the dark

current reduction mechanism was not explored at that time. Hence, future work could focus on studying the dark current draining mechanism in such design to potentially increase its effectiveness.

V. Summary and Conclusion

TID effects have been studied in radiation hardened CMOS Image Sensors and their ability to capture color images with acceptable degradation has been confirmed up to 10 Megagray (1 Gigarad), which represents a sensor radiation hardness improvement compared to previous work [2], [3], [18], [22]–[24]. This work shows that on the studied technology, beyond 1 MGy, 3.3 V N-MOSFETs allow reaching better readout chain performances after irradiation than 1.8 V N and P transistors, thanks to a saturation of the main degradation mechanism in 3.3 V N-channel devices. Hence, despite their thicker oxide, 3.3 V N-MOSFETs appear to be the best choice for designing a simple radiation hardened CIS readout chain.

This work also clarified the influence of several parameters of the radiation hardened photodiode design on its performances after exposure to several Megagray of TID. Especially, the use of thin gate oxide to harden the diode instead of thick gate oxide did not bring significant improvement (less than 10%) and reducing the overlap distance between the protecting gate and the metallurgical junction slightly increased the radiation induced dark current showing that a minimum overlap distance is required. On the other hand, the dark current draining mechanism reported in [3] allowed reducing the dark current by more than a factor of 3 compared to the reference radiation hardened pixel design. Further analysis of this physical process allowed demonstrating that it is a real dark current cancellation phenomenon, not just a simple skimming or an offset compensation. Pixel design variations to benefit further from it will be explored in future work.

Concerning the two photodiode doping profiles studied here, the shallow diode suffers from dark current electric field enhancement after irradiation when 3.3 V operating voltages are used and the deep diode profile is recommended for 3.3 V rad-hard CIS architecture. On the other hand, the shallow diode remains the photodetector of choice for 1.8 V pixels since it yielded the lowest absolute room temperature dark current level reported so far at TID higher than 1 MGy.

In the end, both 1.8 V and 3.3 V architectures are suitable for the design of Megagray-rad-hard-CIS, each with their benefits and limitations, and the final choice depends on the application main requirements.

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